# 36 GHz Dual-Modulus Prescaler in SiGe Bipolar Technology

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***Abstract*** **This paper presents a dual-modulus prescaler with divide ratios of 256 and 257. The circuit uses static divider stages and differential current-mode logic. AND-gates are merged with flip-flops to achieve high operating frequencies at low power consumption. The prescaler operates with input frequencies ranging from below 1 GHz up to 36.4 GHz. It consumes 34.2 mA from a 3 V supply. The circuit is manufactured in a 0.4 $\mu$m SiGe bipolar technology.**

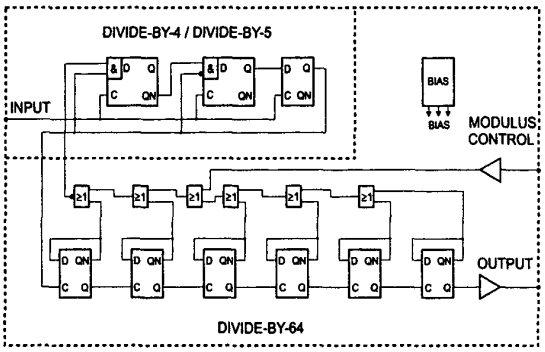


Fig. 1. Prescaler block diagram

## I. Introduction

Dual-modulus prescalers are widely used in frequency synthesizers. They are frequency dividers with two selectable divide ratios and are used to extend the frequency range of programmable dividers. For this application two divide ratios differing by one (P and P+1) are desirable.

The highest frequency reported so far for dual-modulus prescalers is 27 GHz. The circuit is manufactured in GaAs heterojunction FET technology and has divide ratios of 256 and 258 [1]. It uses a divide-by-two input stage and therefore can only achieve the divide ratios of P and P+2 instead of the desired P and P+1. The power consumption of this circuit is 151 mW. For frequencies below 20 GHz prescalers with much lower power consumption have been demonstrated in SiGe [2], [3] and GaAs heterojunction FET [4] technologies.

It was the aim of this work to design a dual-modulus prescaler with divide ratios of 256 and 257 capable of operation above 30 GHz while maintaining low power consumption.

## II. Circuit Design

The prescaler is based on a widely-used architecture [5], [6] and consists of a synchronous divide-by-four/divide-by-five input stage. This stage is followed by an asynchronous six-stage divider with a divide ratio of 64 (figure 1). The overall divider ratio is 256 or 257, depending on the level of the Modulus Control signal.

The maximum operating frequency of the prescaler is determined by the synchronous divider in the input stage. This divider consists of three flip-flops and requires two additional gates in the signal path to allow selection of the divide ratio. These gates result in a reduction of the maximum operating frequency compared to a conventional divider with fixed divide ratio. To achieve a high maximum operating frequency the AND gates are merged with the flip-flops (figure 2). This leads to an increase of the operating speed compared to previous circuits [2]. At the same time the power consumption is reduced because the two current sources required for the separate AND gates can now be omitted.

A further increase of the operating speed is achieved



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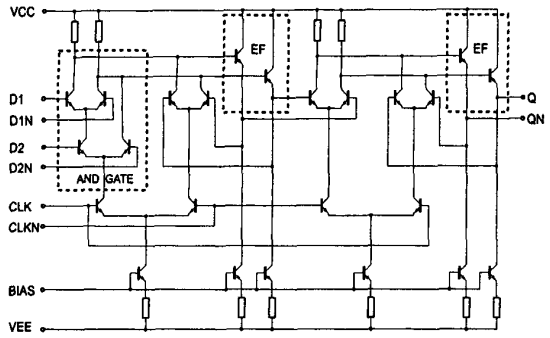


Fig. 2. Master-slave flip-flop with AND gate

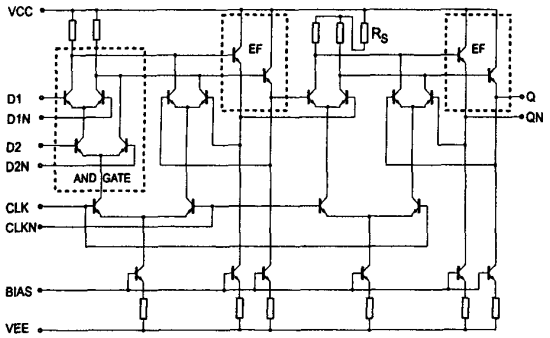


Fig. 3. Master-slave flip-flop with additional resistor $R_S$ for level shifting

by using emitter followers (EF) in the flip-flops. These emitter followers result in an increase of the required minimum supply voltage by one base-emitter voltage $V_{BE}$. Normally, merging the AND gates with the flip-flops requires a further increase of the supply voltage by an additional $V_{BE}$ because there is one additional level of series gating. The resulting high supply voltage would lead to a large increase of the power consumption of the prescaler. Therefore we use resistive level shifting by an amount of $V_{BE}/2$. This allows to implement the additional level of series gating without the need to increase the supply voltage.

Figure 3 shows a flip-flop with an additional resistor $R_S$ for level shifting connected in series to the load resistors. The dc voltage across this resistor is determined by the tail current of the latch and is approximately 400 mV. The common mode level of the differential output signal Q, QN is shifted by this amount. Therefore this output can be directly connected to the input D2, D2N of the merged AND-gate/flip-flop (figure 2) without the need of an additional emitter follower. This allows operation of the prescaler with supply voltages down to 3 V.

The asynchronous divider operates at frequencies that are a factor of four or five lower than the input frequency of the prescaler. Therefore standard current-mode logic (CML) flip-flops without emitter followers can be used. This results in a reduced power consumption because only two current sources are required for each CML flip-flop instead of six current sources in the high-speed flip-flops.

Differential signals are used throughout the prescaler to achieve high noise immunity with a voltage swing of only $2 \times 200$ mV. The input sensitivity of the prescaler is sufficient without an additional amplifier at the input. The single-ended output stage of the prescaler is designed to drive capacitive loads efficiently. A bias network generates the bias voltages for the current sources used in all flip-flops.

## III. Technology

The circuit is fabricated in a pre-production 0.4 $\mu$m-SiGe bipolar technology [7] using a double-polysilicon self-aligned emitter-base configuration with effective emitter width of 0.2 $\mu$m. The maximum transit frequency $f_T$ of the transistors is 85 GHz and the maximum oscillation frequency $f_{max}$ is 128 GHz.

Four layers of aluminum metallization are available. In the prescaler the two lower layers are used for ground and supply planes and for the internal connections of the flip-flops and gates. Connections between these blocks and connections to the pads are made using the two upper metal layers. Fig. 4 shows the chip photograph of the dual-modulus prescaler. The chip size is 550 $\mu$m by 450 $\mu$m.

## IV. Experimental Results

The prescalers were mounted on ceramic substrates with a size of 30 mm $\times$ 30 mm for all measurements (figure 5). Hybrid couplers were used to provide the differential input signal for the prescaler.

The circuit is capable of broadband operation with the minimum frequency limited only by the slew rate of the input signal. The maximum operating frequency is 36.4 GHz. This is the highest operating frequency reported so far for dual-modulus prescalers. Figure 6 shows the measured input sensitivity of the prescaler.

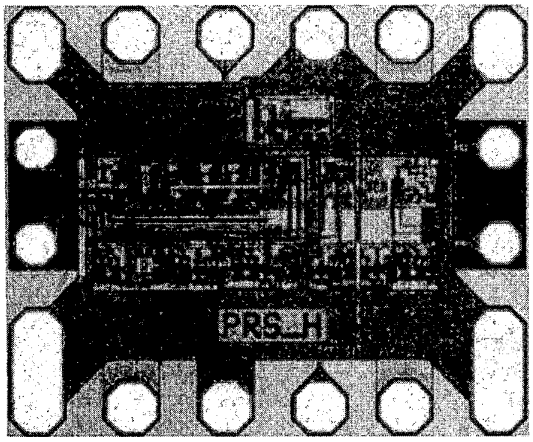


Fig. 4. Chip photograph (size: 550 $\mu$m × 450 $\mu$m)

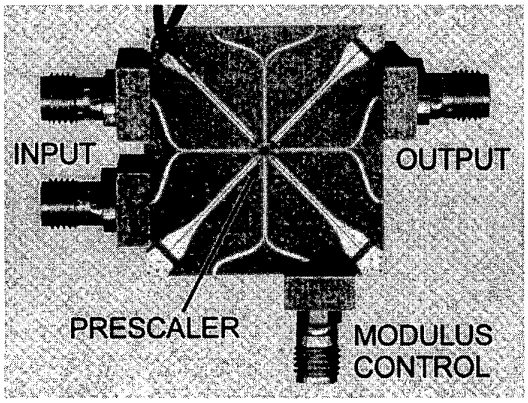


Fig. 5. Prescaler module (30 mm × 30 mm)

This measurement includes the loss caused by bond wires, ceramic substrate, and connectors.

Figure 7 shows the single-ended output signal for an input frequency of 36 GHz and a divide ratio of 256. The output voltage swing of the prescaler is 1.7 $V_{pp}$. This measurement was performed with an external load capacitance of 8 pF at the prescaler output.

The circuit operates from a supply voltage of 3 V and draws 34.2 mA. The power consumption is lower than that reported for previous prescalers which operate at lower frequencies [1]. Table I gives a summary of the prescaler data and table II shows a comparison of this circuit with previously published prescalers.

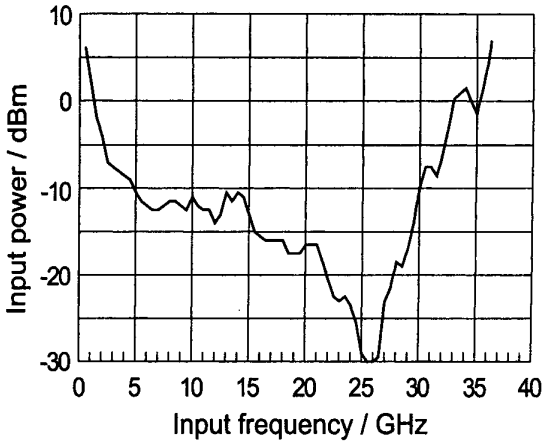


Fig. 6. Measured input sensitivity

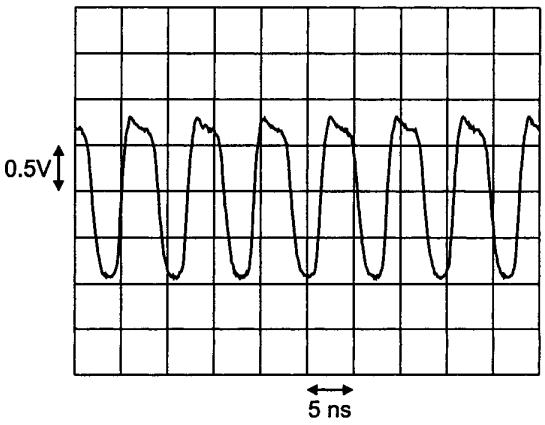


Fig. 7. Output voltage ($f_{IN}$ = 36 GHz, divide ratio 256)

| | |
|---|---|
| Maximum input frequency | 36.4 GHz |
| Output voltage | > 1.5 $V_{pp}$ |
| Divide ratios | 256 / 257 |
| Supply voltage | 3 V |
| Supply current | 34.2 mA |
| Chip size | 550 × 450 $\mu m^2$ |
| Technology | 0.4 $\mu$m SiGe bipolar |

TABLE I. Technical data

| | Maeda 1999 [4] | Knapp 2000 [2] | Wada 1998 [1] | This work |
|---|---|---|---|---|
| Maximum input frequency | 14.5 GHz | 20 GHz | 27 GHz | 36 GHz |
| Power consumption | 22 mW | 27 mW | 151 mW | 103 mW |
| Divide ratios | 256 / 258 | 256 / 257 | 256 / 258 | 256 / 257 |
| Technology | GaAs HJFET | SiGe bipolar | GaAs HJFET | SiGe bipolar |

TABLE II. Comparison of high-speed dual-modulus prescalers

## V. Conclusions

We have presented a dual-modulus prescaler with divide ratios of 256 and 257 manufactured in a 0.4 $\mu$m SiGe bipolar technology. The maximum operating frequency of over 36 GHz is new state of the art. The high operating frequency was achieved with a power consumption of only 103 mW.

## References


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